directing said power signal to said plurality of terminal nodes using an H-tree network, said H-tree network including at least one level, wherein a first level is coupled to said primary input and a last level includes said plurality of terminal nodes for supplying said power signal to a plurality of devices, each of said at least one level having a plurality of segments, each segment of a respective plurality is equal in length; and

wherein a number of segments from said primary input to each of said terminal nodes is equal.

REMARKS

In the Office Action, the Examiner noted that claims 1-11 are pending in the application and that claims 1-11 stand rejected. By this response claims 1, 7, and 10 are amended and claims 2-6, 8-9, and 11 continue un-amended. As per our telephone conversation of November 20, 2002, claims 1, 7, and 10 are being amended to more clearly define the invention and not in response to prior art.

In view of the above amendments and the following discussion, the Applicant respectfully submits that none of the claims now pending in the application is anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Thus, the Applicant believes that all of these claims are now in allowable form.

A. 35 U.S.C. § 102(b)

The Examiner rejected claims 1-5 and 10-11 under 35 U.S.C. § 102(b) as being anticipated by Watanabe et al., U.S. Patent 5,309,001. The rejection is respectfully traversed.

Claim 1

The Examiner alleges that Watanabe et al. discloses a network Fig. 12a for distributing a power signal in an optoelectronic circuit 350 comprising a

plurality of electrically conductive pathways forming at least one level, wherein the portions of the conductive pathways are interconnected; a plurality of segments 353a-353b forming each level, wherein each segment of the level is equal in length; means for coupling 347/352 the power signal from a primary input to a point at the center of a first level; terminal nodes 359a-b coupled at the extremities of a last level for supplying the power signal to devices that form at least a portion of the optoelectronic circuit 350; and wherein the number of segments connecting the primary input to each of the terminal nodes is equal. The Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrik Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)) (emphasis added).

Watanabe et al. teaches a surface electrode on the surface of an LED, wherein the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches. (See Watanabe et al., ABSTRACT). Watanabe et al. fails, though, to disclose at least the invention of the Applicant's claim 1 as follows:

> "A network for distributing a power signal in an optoelectronic circuit, said network comprising:
> a plurality of electrically conductive pathways forming at least one level, wherein portions of said conductive pathways are interconnected;
> a plurality of segments forming each level, wherein each segment of a level is equal in length;
> means for coupling said power signal from a primary input to a point at the center of a first level;
> terminal nodes coupled at the extremities of a last level for supplying said power signal to a ***plurality of devices*** that form at least a portion of said optoelectronic circuit; and
> wherein the number of segments connecting said primary input to each of said terminal nodes is equal." (emphasis added).

Within the context of the present invention, the Applicant discloses:

> "Terminal nodes are coupled to the endpoints of the last level of the H-tree. In this manner a conductive pathway is formed form the primary input to each terminal node, with portions of each conductive pathway being shared between two or more terminal nodes." (See Specification, page 7, lines 13-16).
>
> "The first level is coupled to the primary input, at the center of the two horizontal segments of the H pattern. The conductive pathways distribute a power signal to terminal nodes 16 (represented by circles and as further indicated in the upper right hand quadrant for a portion of the terminal nodes of FIG. 3) on VLSI chip 20, wherein the distance from the primary input to each terminal node 16 is equal. In this illustrative example, **each terminal node 16 represents a VCSEL** and its associated driver." (See Specification, page 6, lines 22-29). (emphasis added).

It is evident from the Applicant's claim 1 and the disclosure, that the Applicant's invention is directed at least in part to "terminal nodes coupled at the extremities of a last level for supplying said power signal to a **plurality of devices** that form at least a portion of said optoelectronic circuit." In addition, the Applicant's specification discloses providing uniform power at the terminal nodes for providing said uniform power to a plurality of devices. The Applicant's invention "eliminates small differences in bias voltage to the optoelectronic devices in different locations of the optoelectronic circuit resulting from resistive voltage drops along a conventional linear power supply line." (See Specification, page 5, lines 2-5). In one embodiment of the present invention, the devices were illustrated as VCSELs. The embodiment of the invention in that case was in part directed to ensuring that the threshold currents and voltages of each VCSEL are identical and that each VCSEL in an array is biased identically via the terminal nodes. (See Specification, page 6, lines 10-13). The Applicant further discloses:

> "Although voltage drops are not typically an issue for digital circuits or for low-current analog circuits, they can have a dramatic effect on the output power of optoelectronics devices and, in particular, VCSELs." (See Applicant's Specification, page 5, lines 20-23). However, as will be understood by persons skilled in the art, a VCSEL, for example, has a very sharp dependence on the voltage across the device due to the so-

called sharp light (output-power)-versus-current characteristics of such devices. In particular, the combination of large current requirements for VCSELs and finite resistance of the power supply lines can lead to small supply differences (e.g. bias voltages) to VCSELs in different parts of the array that result in the large differences in light output power." (See Applicant's Specification, page 5, lines 25-31).

It is a purpose of the Applicant's invention, at least in part, and as evident by the Specification and at least the Applicant' s claim 1, to provide a uniform power distribution to a plurality of devices at said terminal nodes.

In contrast to the Applicant's invention, there is absolutely no teaching in Watanabe et al. for "terminal nodes coupled at the extremities of a last level for supplying said power signal to **a plurality devices** that form at least a portion of said optoelectronic circuit." In contrast to the Applicant's invention and specifically with reference to Fig. 12a as pointed out by the Examiner, Watanabe et al. teaches a surface electrode wherein:

"At the ends of the sixth-order branches 358a and 358b, there are provided contact portions 359a and 359b for making ohmic contact with the underlying semiconductor layer 351. Meanwhile, the rest of the surface electrode 347 other than the contact portions 359a and 359b is in a state in which a Schottky barrier are yielded on the surface of the semiconductor layer 351." (See Watanabe et al., col. 16, lines 1-7).

In the invention disclosed in Watanabe et al., the ends of the sixth-order branches and the semiconductor layer are put into ohmic contact via the contact portions, while the rest of the surface electrode and the semiconductor layer are put into a state in which current flow is suppressed, to facilitate an improvement in quantum efficiency of a LED by allowing any light to easily flow out of a LED. (See Watanabe et al., col. 16, lines 38-50). The terminal nodes of the Applicant's invention are not and cannot be in ohmic contact with an underlying layer for the invention to function as disclosed.

In addition, Watanabe et al. is directed to and teaches the reduction of ineffective light emission of a **single** LED whereby the surface electrode and the

semiconductor layer are in electrical contact with each other at ends of the highest-order branches for providing power to said **single** LED. (See Watanabe et al., Abstract). There is absolutely no teaching in Watanabe et al. for supplying a power to a **plurality of devices** as claimed in at least the Applicant's claim 1.

Therefore, the Applicant submits that claim 1 is not anticipated by the teachings of Watanabe et al. and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise independent claim 10 recites similar relevant features as those recited in claim 1. As such, the Applicant respectfully submits that claim 10 is also not anticipated by the teachings of Watanabe et al. and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 2-5 and 11 depend directly from claims 1 and 10, respectively, and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that none of these claims are anticipated by the teachings of Watanabe et al. Therefore the Applicant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

B. 35 U.S.C. § 103(a)

The Examiner rejected claims 6-9 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe et al., U.S. Patent 5,309,001, in view of Olbright et al., U.S. Patent 5,266,794/Schneider et al., U.S. Patent 5,351,256/Lebby et al., U.S. Patent 5,337,397. The rejection is respectfully traversed.

Claim 6

Claim 6 depends directly from independent claim 1 and recites limitations thereof. The Examiner applied Watanabe et al. to claim 6 as described above for the Examiner's rejection of claim 1. The Examiner alleges that Watanabe et al. teach all of the stated limitations except for the integrated circuits are VCSELs;

instead Watanabe et al. teach the integrated circuits are LEDs. The Applicant respectfully disagrees that Watanabe et al. teach all of the stated limitations except for the integrated circuits are VCSELs.

The Applicant does agree with the Examiner, though, that Watanabe et al. does not teach that the integrated circuits are VCSELs.

As described above, the teachings of Watanabe et al. do not suggest or describe at least the Applicants' invention at least with regard to claim 1 for "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit."

Furthermore, the teachings of Olbright et al., Schneider et al., or Lebby et al., alone, do not teach, suggest, or describe the invention of the Applicant, at least with regard to claim 1. Neither Olbright et al., Schneider et al., nor Lebby et al., teach or suggest "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit."

The Applicant further submits that there is no suggestion or motivation to combine the teachings of Watanabe et al. and the teachings of Olbright et al., Schneider et al., or Lebby et al.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984);

The Applicant further submits that even if there was a motivation or suggestion to combine the references (which the Applicant believes that there is none), the teachings of Olbright et al., Schneider et al., and Lebby et al., either alone or in any allowable combination, fail to bridge the substantial gap between the Applicant's invention, and the teachings of Watanabe et al.

The Examiner further alleges that it is well known in the laser art that one may use either laser source (e.g. LED or VCSEL) as a matter of obvious design choice, see Olbright et al. col. 8, lines 65-68/Schneider et al. col. 1, lines 14-16/Lebby et al. col. 3, lines 17-27. The Applicant respectfully disagrees.

The suggestion by the Examiner that the function of an LED is interchangeable with the function of a VCSEL in no way renders obvious a network for distributing a power signal wherein, "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit" as claimed in the Applicant's claim 1, in light of a surface electrode on the surface of a LED, wherein the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches, as disclosed in Watanabe et al. It is true that an LED may be interchangeable with a VCSEL in some applications when using said devices as lights sources, but the powering requirements or powering methods for an LED and a VCSEL are not similar at all. As stated above, the Applicant's invention is, at least in part, directed to powering a plurality of devices, such as VCSELs, that benefit in operation when receiving a uniform bias voltage among the plurality of devices. As such, to allege that one may use either a laser source (e.g. LED or VCSEL) as a matter of

obvious design choice in this capacity (i.e. powering requirements) would be an incorrect statement or analogy.

As such, and at least for the reason that neither Olbright et al., Schneider et al., nor Lebby et al., alone or in any combination with Watanabe et al., do not teach suggest, or describe the Applicants' invention with regard to claim 1, the Applicants respectfully submit that dependent claim 6 is also not rendered obvious by Watanabe et al. in view of Olbright et al., Schneider et al., or Lebby et al.

Therefore, the Applicant submits that claim 6 as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Claims 7-9

The Examiner alleges that regarding claims 7-9, Watanabe et al. teach all the stated limitations except for the plurality of electrically conductive pathways being separate; instead, Watanabe et al. teach the pathways being formed of wider/broader pathways that diverge as it branches to a higher level/order. The Applicants respectfully disagree.

Claim 7 is an independent claim that recites similar relevant features as those recited in claim 1. As described above with regard to the Examiner's rejection of claim 1, the teachings of Watanabe et al. do not teach, suggest or describe at least the Applicants' invention with regard to claim 1 for "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit." As independent claim 7 recites similar relevant features as those recited in claim 1, the Applicant respectfully submits that the teachings of Watanabe et al. also do not teach, suggest or describe at least the Applicants' invention with regard to claim 7.

Furthermore, the teachings of Olbright et al., Schneider et al., or Lebby et al., alone, do not teach, suggest, or describe the invention of the Applicant, at least with regard to claim 1. Neither Olbright et al., Schneider et al., nor Lebby et

al., teach or suggest "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit."

The Applicant further submits that there is no suggestion or motivation to combine the teachings of Watanabe et al. and the teachings of Olbright et al., Schneider et al., or Lebby et al. Even if there was a motivation or suggestion to combine (which the Applicant believes that there is none), the teachings of Olbright et al., Schneider et al., and Lebby et al., either alone or in any allowable combination, fail to bridge the substantial gap between the Applicant's invention, and the teachings of Watanabe et al.

Therefore, the Applicant submits that claim 7 as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Furthermore, dependent claims 8 and 9 depend directly from claim 7 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that none of these claims are obvious with respect to the teachings of Watanabe et al. Therefore the Applicant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Applicants' Note

The Applicant would like to thank the Examiner for his assistance and suggestions in the furtherance of this application. As per our telephone conversation of November 20, 2002 claims 1, 7, and 10 are being amended to more clearly define the invention and not in response to prior art. The Applicant also respectfully submits that the amendments to claims 1, 7, 10 do not constitute new matter.

Conclusion

Thus the Applicant submits that none of the claims, presently in the application, are anticipated under the provisions of 35 U.S.C. § 102 or obvious

under the provisions of 35 U.S.C. § 103. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

E/Wall

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Dated: 11/25/02

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MARKED UP CLAIMS

1. (Amended) A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of electrically conductive pathways forming at least one level, wherein portions of said conductive pathways are interconnected;

a plurality of segments forming each level, wherein each segment of a level is equal in length;

means for coupling said power signal from a primary input to a point at the center of a first level;

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit; and

wherein the number of segments connecting said primary input to each of said terminal nodes is equal.

7. (Amended) A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of separate electrically conductive pathways forming at least one level, wherein said pathways are joined only at a common point;

a plurality of segments forming each level, wherein each segment of a level is equal in length;

means for coupling said power signal from a primary input to a point at the center of a first level;

terminal nodes coupled at the extremites of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit; and

wherein the number of segments connecting said primary input to each of said terminal nodes is equal.

10. (Amended) A method of distributing a power signal to a plurality of terminal nodes on an optoelectronic circuit, the method comprising the steps of:

receiving the power signal form a primary input; and

directing said power signal to said plurality of terminal nodes using an H-tree network, said H-tree network including at least one level, wherein a first level is coupled to said primary input and a last level includes said plurality of terminal nodes for supplying said power signal to a plurality of devices, each of said at least one level having a plurality of segments, each segment of a respective plurality is equal in length; and

wherein a number of segments from said primary input to each of said terminal nodes is equal.